

endurance limit is approximately 10^6 program/erase cycles. In a ten-year projected life time of the device, this translates to a limit of one program/erase cycle per 5 minutes. This may be marginal in normal computer usage.

IN THE CLAIMS:

Please cancel the original parent application claims 1-62, without prejudice, and substitute the following new claims therefore:

① --63. A defect management engine comprising:
a memory array comprising a plurality of groups of data cells and address cells,
said cells in each of said groups of data cells and address cells respectively storing data and addresses;
means for accessing at least one of said plurality of groups of data cells and address cells;
means for detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address; and
means for outputting data from said accessed group of data cells when said address match condition is detected.

64. The defect management engine as recited in claim 63, further comprising at least one main memory wherein said data cells are redundancy data cells for replacing defective ones of said data cells in said at least one main memory, and said address cells are redundancy address cells for storing addresses of defective ones of data cells in said at least one main memory.

65. The defect management engine as recited in claim 63 further comprising means for overriding said accessed group of data cells respectively with new data, when said address match condition is detected.

66. The defect management engine as recited in claim 63, wherein said data cells and said address cells are of a same cell type.

67. The defect management engine as recited in claim 63, wherein addresses stored in said address cells are non-volatile.

68. The defect management engine as recited in claim 63 further comprising means for programming addresses stored in said address cells.

69. The defect management engine recited in claim 64, wherein said redundancy data cells are of a same cell type as said data cells in said at least one main memory

70. The defect management engine as recited in claim 68, wherein said means for programming is enabled by a command generated by a controller means.

71. The defect management engine as recited in claim 68, wherein said means for programming replicates said addresses into said address cells by sequentially activating each of said address cells.

72. The defect management engine as recited in claim 68, wherein said means for programming replicates said addresses into said address cells by simultaneously activating at least two of said address cells.

73. The defect management engine as recited in claim 64 further comprising means for enabling a single-bit and a multi-bit redundancy replacement within said at least one main memory.

74. The defect management engine as recited in claim 73, wherein said multi-bit size redundancies replace multiple defective ones of said data cells within said at least one main memory with one group of said plurality of groups of redundancy data cells

75. The defect management engine as recited in claim 73 further comprising means for enabling a variable bit size redundancy replacement in said at least one main memory.

76. The defect management engine as recited in claim 64, wherein said data cells are redundancy data cells for replacing defective ones of said data cells present in at least one domain within said at least one main memory, and said address cells are redundancy address cells for addressing defective ones of said data cells within said at least one domain.

77. The defect management engine as recited in claim 76, wherein said plurality of groups of redundancy data cells and redundancy address cells is assigned to said at least one domain.

78. The defect management engine as recited in claim 76, wherein said at least one domain within said at least one main memory is supported by at least one of said plurality of groups of redundancy data cells and redundancy address cells.

79. The defect management engine as recited in claim 63, wherein said means for accessing at least one of said plurality of groups includes wordline drivers.

80. The defect management engine as recited in claim 79, wherein said means for accessing at least one of said plurality of groups further includes sense amplifiers.

81. The defect management engine as recited in claim 79, wherein said wordline driver enables means for assigning to said plurality of groups of data cells and address cells respective redundancy ones of said redundancy data cells and redundancy address cells to repair a plurality of faults in at least one of said domains.

82. A defect management engine coupled to at least one main memory comprising:

a memory array comprising a plurality of groups of redundancy data cells and redundancy address cells, said cells in each of said groups of redundancy data cells and redundancy address cells respectively storing redundancy data and redundancy addresses;

means for accessing at least one of said plurality of groups of redundancy data cells and redundancy address cells;

means for detecting a redundancy address match condition for each of said accessed groups, wherein the redundancy address of said accessed group matches one of a plurality of inputted addresses; and

means for outputting redundancy data from said accessed group of redundancy data cells and redundancy address cells when said redundancy address match condition is detected.

83. The defect management engine as recited in claim 82 further comprising means for overriding said accessed group of redundancy data cells with new data when said redundancy address match condition is detected.

84. The defect management engine as recited in claim 82, wherein said redundancy data cells and said redundancy address cells are of a same cell type

85. A defect management system comprising a plurality of memory chips, and at least one defect management engine chip coupled to each of said memory chips, said at least one defect management engine chip comprising:

a memory array comprising a plurality of groups of data cells and address cells, said cells in each of said groups of data cells and address cells respectively storing data and addresses;

means for accessing at least one of said plurality of groups of data cells and address cells;

means for detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address; and

means for outputting data from said accessed group of data cells when said address match condition is detected.

86. The defect management system as recited in claim 85 further comprising a non-volatile random access memory chip coupled to each of said memory chips.

40 87. A defect management system comprising a plurality of chips, each of said chips comprising at least one memory, and at least one defect management engine coupled to said at least one memory, said at least one defect management engine comprising: a memory array comprising a plurality of groups of data cells and address cells, said cells in each of said groups of data cells and address cells respectively storing data and addresses; means for accessing at least one of said plurality of groups of data cells and address cells; means for detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address; and means for outputting data from said accessed group of data cells when said address match condition is detected.

88. The defect management system as recited in claim 87 further comprising at least one non-volatile random access memory coupled to said at least one memory and to said at least one defect management engine.

43 89. A defect management system comprising a plurality of chips, each of said chips comprising at least one memory, at least one non-volatile random access memory coupled to said at least one memory, and at least one defect management engine coupled to said at least one memory, said at least one defect management engine comprising: a memory array comprising a plurality of groups of data cells and address cells, said cells, in each of said groups of data cells and address cells respectively storing data and addresses; means for accessing at least one of said plurality of groups of data cells and address cells; means for detecting an address match condition for each of said accessed groups, wherein the address of said accessed group matches an inputted address; and means for outputting data from said accessed group of data cells when said address match condition is detected.

90. The defect management system as recited in claim 89 further comprising at least one defect management engine chip coupled to each of said chips comprising said at least one memory and to said at least one non-volatile random access memory.

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91. A method of managing defects comprising the steps of:
 configuring a memory array in a plurality of groups of data cells and
 address cells, said cells in each of said groups of data cells and address cells respectively
 storing data and addresses;
 accessing at least one of said plurality of groups of data cells and address
 cells;
 detecting an address match condition for each of said accessed groups,
 wherein the address of said accessed group matches one of a plurality of inputted
 addresses; and
 outputting data from said accessed group of data cells and address cells
 when said address match condition is detected.

92. The method of managing defects as recited in claim 91 further comprising the
step of overriding with new data said accessed group of data cells when said address
match condition is detected.

93. The method of managing defects as recited in claim 91, wherein said data
cells and said address cells are of a same cell type.

94. The method of managing defects as recited in claim 91, wherein the addresses
stored in said address cells are non-volatile.

95. The method of managing defects as recited in claim 91 further comprising
means for programming said addresses stored in at least one of said address cells.

96. A method of managing defects comprising the steps of:
 configuring a memory array into a plurality of groups of redundancy data
 cells and redundancy address cells, said cells respectively storing redundancy data and
 redundancy addresses;